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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/608,390	06/26/2003	Tak M. Mak	884.833US1	8383

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SIDDIQUI, SAQIB JAVAID	

ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 05/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/608,390	MAK ET AL.	
	Examiner	Art Unit	
	Saqib J. Siddiqui	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *21 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Applicant's response was received and entered February 21, 2006.

- Claims 1-26 are pending. Claims 1-3, 7, 10, 12, 18, & 24 are amended.
- Application is currently pending.

Specification

The corrections to the specification were received on February 21, 2006. The Abstract is now acceptable. The previous objections are hereby withdrawn

Claim Objections

The corrections to the claims were received on February 21, 2006. These claims are now acceptable. The previous objections are hereby withdrawn.

Claim Rejections - 35 USC § 112

The corrections to the claims were received on February 21, 2006. These claims are now acceptable. The previous *35 USC § 112* rejections are hereby withdrawn.

Response to Amendment

Applicant's arguments and amendments with respect to amended claims 1-3, 7, 10, 12, 18, & 24 and previously presented claims 2, 4-6, 8-9, 11, 13-17, 19-23, & 25-26 filed February 21, 2006 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-26 are rejected under 35 U.S.C. 103 (a) as being unpatented over Kundu et al. US 6,510,398 B1 and further in view of Evans US PG Pub no. 20030051197 A1.

As per claim 1:

Kundu et al. substantially teaches a method, comprising acquiring test data from a testing device (Figure 1 # 110, column 3, lines 44-48), loading at least a portion of the test data to a cache onto a device under test (Figure 1 # 130, columns 3-4, lines 66-3), processing the portion of the test data in the cache on the device under test (Figure 1 # 140, column 4, lines 4-6), and intercepting requests associated with other data falling outside of the cache by a pseudo bus agent to emulate a bus operation for an intercepted request (Figure 1 # 160, column 4, lines 7-12).

Kundu et al. does not explicitly teach wherein the emulated bus operation reflects a test associated with a cache page operation of the cache.

However, Evans in an analogous art teaches the emulated bus operation reflects a test associated with a cache page operation of the cache (Figure 1, paragraph [0011-0037]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to enable Kundu et al.'s invention to be able to test cache, since one of ordinary skill in the art would have realized that enabling Kundu et al.'s invention to test the cache page would have provided the efficiency for testing the cache in a single operation instead of requiring separate tests for the RAM and the CAM causing

the invention to be cost effective, and decreasing the need for an external or separate tester (Evans, paragraph [0010]). Further it should be noted that Kundu et al.'s invention is for testing integrated circuits during manufacturing using built in circuitry (Kundu et al., column 1, lines 5-15). Evans's invention also allows the integrated circuits (ICs) incorporating the cache memories to perform tests of the cache memories, for verification testing during IC manufacture (paragraph [0003]). Hence, it is apparent that enabling Kundu et al.'s invention to test the cache will only make the testing process more efficient.

As per claim 2:

Kundu et al./Evans teaches a method of claim wherein providing includes deterministically or randomly generating the pseudo-test data by the pseudo bus agent (Figure 1 # 110, column 3, lines 44-48).

As per claim 3:

Kundu et al./Evans teaches a method wherein providing includes acquiring the pseudo test data by selecting a data source within the device under test (Figure 1 # 120, column 3, lines 50-55).

As per claim 4:

Kundu et al./Evans teaches a method further comprising compressing results associated with the processing and the intercepting on the device under test (Figure 1 # 170, column 4, lines 24-27).

As per claim 5:

Kundu et al./Evans teaches a method further providing the compressed results to the testing device by the device under test (Figure 1 # 175, column 4, lines 29-31).

As per claim 6:

Kundu et al./Evans teaches a method wherein compressing includes representing the compressed results as a digital signature for the test data (Figure 1 # 170, column 4, lines 24-27).

As per claim 7:

Kundu et al. substantially teaches a method, comprising sending test data to a device under test (Figure 1 # 130, columns 3-4, lines 66-3), receiving from the device under test a signature associated with results of the test data (Figure 1 # 175, column 4, lines 29-31), and validating the signature against an expected signature (Figure 1 # 180, column 4, lines 32-39).

Kundu et al. does not explicitly teach the method wherein at least a portion of the results is associated with testing an emulation of a cache paging operation associated with a cache of the device under test.

However, Evans in an analogous art teaches the method wherein at least a portion of the results is associated with testing an emulation of a cache paging operation associated with a cache of the device under test (Figure 1, paragraph [0011-0037]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to enable Kundu et al.'s invention to be able to test cache, since one of ordinary skill in the art would have realized that enabling Kundu et al.'s invention to test the cache page would have provided the efficiency for testing the cache in a

single operation instead of requiring separate tests for the RAM and the CAM causing the invention to be cost effective, and decreasing the need for an external or separate tester (Evans, paragraph [0010]). Further it should be noted that Kundu et al.'s invention is for testing integrated circuits during manufacturing using built in circuitry (Kundu et al., column 1, lines 5-15). Evans's invention also allows the integrated circuits (ICs) incorporating the cache memories to perform tests of the cache memories, for verification testing during IC manufacture (paragraph [0003]). Hence, it is apparent that enabling Kundu et al.'s invention to test the cache will only make the testing process more efficient.

As per claim 8:

Kundu et al./Evans teaches a method further comprising using a pseudo bus agent, by the device under test, to emulate data traffic on a bus of the device under test when the test data is processed on the device under test (Figure 1 # 160, column 4, lines 7-15).

As per claim 9:

Kundu et al./Evans teaches a method further comprising storing, by the device under test, at least a portion of the test data in a cache on the device under test (Figure 1 # 130, columns 3-4, lines 66-3).

As per claim 10:

Kundu et al./Evans teaches a method wherein storing includes servicing requests, by the pseudo bus agent, for other data residing outside the cache by providing responses back to the cache (Figure 1 # 120, column 3, lines 50-65).

As per claim 11:

Kundu et al./Evans teaches a method wherein receiving includes representing the signature as a compressed version of the results (Figure 1 # 175, column 4, lines 29-31).

As per claim 12:

Kundu et al. substantially teaches a system, comprising a cache (Figure 2 # 270, column 5, lines 1-5), a pseudo bus agent (Figure 1 # 160, column 4, lines 7-22), and a processor for executing instructions associated with test data in the cache (Figure 1 # 140, column 4, lines 4-6), wherein the test data is received from a testing device and the pseudo bus agent emulates responses from a bus as if the responses had originated from the bus during the execution of the test data (Figure 1 # 160, column 4, lines 7-22).

Kundu et al. does not explicitly teach the system wherein at least one response emulated reflects a cache page operation associated with the cache.

However, Evans in an analogous art teaches the system wherein at least one response emulated reflects a cache page operation associated with the cache (Figure 1, paragraph [0011-0037]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to enable Kundu et al.'s invention to be able to test cache, since one of ordinary skill in the art would have realized that enabling Kundu et al.'s invention to test the cache page would have provided the efficiency for testing the cache in a single operation instead of requiring separate tests for the RAM and the CAM causing the invention to be cost effective, and decreasing the need for an external or

separate tester (Evans, paragraph [0010]). Further it should be noted that Kundu et al.'s invention is for testing integrated circuits during manufacturing using built in circuitry (Kundu et al., column 1, lines 5-15). Evans's invention also allows the integrated circuits (ICs) incorporating the cache memories to perform tests of the cache memories, for verification testing during IC manufacture (paragraph [0003]). Hence, it is apparent that enabling Kundu et al.'s invention to test the cache will only make the testing process more efficient.

As per claim 13:

Kundu et al./Evans teaches a system wherein the pseudo bus agent generates deterministic or random data to emulate the responses from the bus (Figure 1 # 110, column 3, lines 42-47).

As per claim 14:

Kundu et al./Evans teaches a system wherein the pseudo bus agent selects data from a variety of data sources to emulate the responses from the bus (Figure 1 # 160, column 4, lines 7-22).

As per claim 15:

Kundu et al./Evans teaches a system wherein processor logic generates a signature for test data results (Figure 1 # 170, column 4, lines 23-30).

As per claim 16:

Kundu et al./Evans teaches a system wherein the bus is in communication with the testing device (column 4, lines 66-3).

As per claim 17:

Kundu et al./Evans teaches a system wherein the test data includes instruction data (Figure 1 # 120, column 3, lines 50-65).

As per claim 18:

Kundu et al. substantially teaches a machine accessible medium having associated data (Figure 2 # 230, column 5, lines 11-16), which when accessed, results in a machine performing receiving a request for data on the bus (Figure 1 # 130, columns 3-4, lines 66-3) in order to service a cache of the machine (Figure 2 # 270, column 5, lines 1-5), generating pseudo data in response to the request (Figure 1 # 110, column 3, lines 43-47), and providing the pseudo data in the cache to satisfy the request (Figure 2 # 270, columns 5-6, lines 67-4).

Kundu et al. does not explicitly teach the machine accessible medium wherein at least a portion of the pseudo data reflects a response for testing a cache page operation associated with the cache of the machine.

However, Evans in an analogous art teaches the machine accessible medium wherein at least a portion of the pseudo data reflects a response for testing a cache page operation associated with the cache of the machine (Figure 1, paragraph [0011-0037]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to enable Kundu et al.'s invention to be able to test cache, since one of ordinary skill in the art would have realized that enabling Kundu et al.'s invention to test the cache page would have provided the efficiency for testing the cache in a single operation instead of requiring separate tests for the RAM and the CAM causing the invention to be cost effective, and decreasing the need for an external or separate

tester (Evans, paragraph [0010]). Further it should be noted that Kundu et al.'s invention is for testing integrated circuits during manufacturing using built in circuitry (Kundu et al., column 1, lines 5-15). Evans's invention also allows the integrated circuits (ICs) incorporating the cache memories to perform tests of the cache memories, for verification testing during IC manufacture (paragraph [0003]). Hence, it is apparent that enabling Kundu et al.'s invention to test the cache will only make the testing process more efficient.

As per claim 19:

Kundu et al./Evans teaches a medium wherein the data further includes data, which when accessed, results in the machine performing acquiring the pseudo data from another resource of the machine (Figure 2 # 230, column 5, lines 10-15).

As per claim 20:

Kundu et al./Evans teaches a medium wherein the data further includes data, which when accessed, results in the machine performing deterministically or randomly generating the pseudo data in the machine (Figure 2 # 240, column 5, lines 34-45).

As per claim 21:

Kundu et al./Evans teaches a medium wherein the data further includes data, which when accessed, results in the machine performing representing the pseudo data as a return value associated with a write operation request (Figure 1 # 170, column 4, lines 23-30).

As per claim 22:

Kundu et al./Evans teaches a medium wherein the data further includes data, which when accessed, results in the machine performing, representing the pseudo data in a format expected by the request having a pseudo data value that represents a deterministic or random data value associated with a read operation request (Figure 1 # 175, column 5, lines 29-32).

As per claim 23:

Kundu et al./Evans teaches a medium wherein the data further includes data, which when accessed, results in the machine performing using the pseudo data to emulate a bus transaction over the bus (column 5, line 34-55).

As per claim 24:

Kundu et al. teaches an apparatus comprising a cache for a device under test (DUT) (Figure 2 # 270, column 5, lines 1-5), and a pseudo bus agent (PBA) (Figure 2 # 240, column 5, lines 35-48), wherein the cache houses instructions for testing the DUT and the PBA services requests generated by a number of executing instructions when bus transactions are needed (Figure 1 # 130, columns 3-4, lines 66-5), the PBA services the requests by emulating the corresponding bus transactions and provides emulated results back to the cache (Figure 1 # 150, column 4, lines 4-6).

Kundu et al. does not explicitly teach the apparatus wherein at least a portion of the results is associated with testing an emulation of a cache paging operation associated with a cache of the device under test.

However, Evans in an analogous art teaches the apparatus wherein at least a portion of the results is associated with testing an emulation of a cache paging

operation associated with a cache of the device under test (Figure 1, paragraph [0011-0037]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to enable Kundu et al.'s invention to be able to test cache, since one of ordinary skill in the art would have realized that enabling Kundu et al.'s invention to test the cache page would have provided the efficiency for testing the cache in a single operation instead of requiring separate tests for the RAM and the CAM causing the invention to be cost effective, and decreasing the need for an external or separate tester (Evans, paragraph [0010]). Further it should be noted that Kundu et al.'s invention is for testing integrated circuits during manufacturing using built in circuitry (Kundu et al., column 1, lines 5-15). Evans's invention also allows the integrated circuits (ICs) incorporating the cache memories to perform tests of the cache memories, for verification testing during IC manufacture (paragraph [0003]). Hence, it is apparent that enabling Kundu et al.'s invention to test the cache will only make the testing process more efficient.

As per claim 25:

Kundu et al./Evans teaches an apparatus wherein the emulated results are compressed into a signature (Figure 1 # 170, column 4, lines 24-30).

As per claim 26:

Kundu et al./Evans teaches the apparatus wherein the DUT sends the signature to a tester when testing is complete for verification (Figure 2 # 250, column 5, lines 34-55).

Related Art

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Additional pertinent prior arts, US 6377065 B1, US 6294921 B1, US 6049901 A, and US 5930735 A mention the same pattern of circuit testing are included herein for Applicant's review.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to the final action is set to expire in THREE MONTH from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of the final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Saqib J. Siddiqui whose telephone number is (571) 272-6553. The examiner can normally be reached on 8:00 to 4:30. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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04/21/2006

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